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PATENT APPLICATION

Do. No. 5038-062

THAT THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: John B. Halbert and Randy M. Bonella

Serial No.: 09/666,528

Examiner: Huan Hoang

Filed:

September 18, 2000

Group Art Unit: 2818

For:

MEMORY SYSTEM HAVING BUFFERS FOR ISOLATING

STACKED MEMORY DEVICES

Date:

February 25, 2002

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Assistant Commissioner for Patents Washington, DC 20231

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:

COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON D.C. 20231

ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON D.C. 20231

ASSISTANT COMMISSIONER FOR FRADEMARKS 2900 CRYSTAL DRIVE ARLINGTON, VA 22202-3513

James to

RESPONSE TO OFFICE ACTION

Responsive to the Office Action, dated October 25, 2001, please amend the application as follows.

03/12/20@2 BNGUYEN1 0000006 09666528

01 FC:103 02 FC:102 03 FC:115 162.00 OP 420.00 OP

IN THE CLAIMS

110.00 OP Please amend the claims by rewriting as follows:

1. (Amended once) A memory system comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices, wherein the buffer is not

stacked with the first and second memory devices.

1.1

(Amended once) A memory module comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus, wherein the buffer is not stacked with the first and second memory devices.

Response to Office Action

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